REMARKS

Claims 1-13, 20, and 31-41 are currently pending in the application. Claims 8-12 and 32-41 were withdrawn from consideration by the Examiner as being directed to a non-elected invention or species. Reconsideration of the rejected claims in view of the following remarks is respectfully requested.

Pending Claims

Applicants note that the Office Action Summary dated 5/2/07 lists claims 1-7, 13, 20, and 31 as pending. However, Applicants note that, in addition to claims 1-7, 13, 20, and 31, withdrawn claims 8-12 and 32-41 are also pending (albeit withdrawn from consideration). Applicants respectfully request clarification of this issue in the next Official communication.

Allowable Subject Matter

Applicants appreciate the indication that claims 2-7 contain allowable subject matter. However, claims 2-7 are not being presented in independent form at this time, because Applicants submit that all of the pending claims are in condition for allowance for the following reasons.

35 U.S.C. §102 Rejection

Claims 1, 13, 20, and 31 are rejected under 35 U.S.C. §102(e) for being anticipated by U.S. Patent Application Publication No. 2003/0219937 issued to Peterson et al. ("Peterson"). This rejection is respectfully traversed.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See MPEP §2131. Applicants submit that the applied art does not show each and every feature of the claimed invention.

As discussed in Applicants' prior response dated February 7, 2007, the present invention relates to a method of (and a substrate for) manufacturing strained and non-strained silicon regions on the same chip. It is known to impart tensile or compressive stress to semiconductor devices to improve device performance. Such stresses may be imparted by forming the devices in areas of strained silicon. However, imparting these stresses may lead to defects in the areas of strained silicon. Defects can be detrimental in that they degrade the performance of defect-sensitive devices (e.g., DRAM devices), and compromise the production yield of defect sensitive devices. Exemplary implementations of the invention avoid such detrimental effects by allowing high-performance logic devices to be made in strained regions of a chip and high-quality, defect-sensitive devices to be made in non-strained regions of the same chip. Independent claim 1 recites:

> 1. A method, comprising:
> forming a pattern of strained material and relaxed material on a substrate;
> forming a strained device in the strained material; and
> forming a non-strained device in the relaxed material.

Moreover, independent claim 31 recites:

> 31. An electrical device, comprising:
> a pattern of strained material and relaxed material formed on a substrate;
> a first device formed in the first strained material; and
> a second device formed in the relaxed material.

The Examiner asserts that Peterson discloses these features at FIG. 1C and Paragraph [0007] (Office Action, page 2). Applicants respectfully disagree, and submit that Peterson does not disclose forming a strained device in the strained material, and forming a non-strained device in the relaxed material, as recited in claim 1; or, a first device formed in the first strained material, and a second device formed in the relaxed material, as recited in claim 31.

Peterson discloses a method for co-fabricating strained and relaxed crystalline and poly-crystalline structures. More specifically, in FIG. 1C, Peterson shows a substrate 102 having a relaxed layer 104 and a strained layer 110 formed thereon. As such, Applicants acknowledge that Peterson discloses forming a pattern of strained material and relaxed material on a substrate, as recited in claim 1, and a pattern of strained material and relaxed material formed on a substrate, as recited in claim 31.

However, Peterson does not disclose forming a strained device in the strained material, and forming a non-strained device in the relaxed material, as recited in claim 1; or a first device formed in the first strained material, and a second device formed in the relaxed material, as recited in claim 31. In fact, Peterson does not disclose any devices whatsoever in FIG. 1C, much less devices formed in the respective layers 104, 110. Instead, Peterson only discloses the strained layer 104 and the relaxed layer 110. This, however, does not constitute forming a strained device in a strained material, or forming a non-strained device in a relaxed material.

Moreover, Applicants submit that Paragraph [0007] of Peterson does not disclose respective devices formed in the respective materials. Applicants acknowledge that Peterson discusses the desirability of having a PMOS device with compressively strained layer. Peterson also separately discusses an NMOS device fabricated over a relaxed layer. However, Petersons's

use of the terms "with" and "over" does not constitute a disclosure that these PMOS and NMOS devices are formed in the layers 104, 110 of FIG. 1C.

Furthermore, Peterson makes no mention whatsoever of strained and non-strained devices, which are recited in the claimed invention. To the contrary, Peterson merely discloses PMOS and NMOS devices in the Background section of the application; however, there is no disclosure that these PMOS and NMOS devices constitute a strained device and a non-strained device. By comparison, exemplary embodiments of the invention describe a strained device as a logic device, and a non-strained device as a memory device (see, for example, Paragraphs [0041] and [0046]), and claims 1 and 31 explicitly recite a strained device and a non-strained device. Peterson, on the other hand, simply does not disclose strained and non-strained devices.

For all of the reasons discussed above, Applicants submit that Peterson cannot reasonably be said to disclose forming a strained device in the strained material, and forming a non-strained device in the relaxed material, as recited in claim 1; or, a first device formed in the first strained material, and a second device formed in the relaxed material, as recited in claim 31. Therefore, Peterson does not anticipate the claimed invention.

Applicants submit that claims 13 and 20 depend from allowable claim 1, and are allowable at least for the reasons discussed above with respect to claim 1.

Accordingly, Applicants respectfully request that the §102(e) rejection of claims 1, 13, 20, and 31 be withdrawn.

Request for Rejoinder of Withdrawn Claims

Applicants request that the Examiner rejoin claims 8-12 and 32-41 and examine these claims on the merits. As discussed above, generic claim 1 is allowable, thus rejoinder and

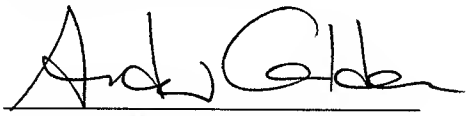
examination of claims 8-12 is proper. Also, because linking claim 31 is allowable for the reasons set forth above, rejoinder and examination of claims 32-41 is proper.

Moreover, as claims 8-12 and 32-41 depend from allowable independent claims, Applicants believe that these claims are patentably distinct from the applied prior art and are in condition for allowance.

CONCLUSION

In view of the foregoing remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0458

Respectfully submitted,
Kangguo CHENG et al.



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